

### **AMENDMENT TO THE TITLE**

Please delete the title in its entirety and please substitute the following:

--METHOD AND DEVICE FOR CONTROLLING THE POWER SUPPLY OF A SUBCONTROLLER USING A MONITORING TASK AND A PREDETERMINED TIME-OUT PERIOD--.

### **AMENDMENTS TO THE SPECIFICATION**

**Please replace the paragraph at page 2, lines 18-21, with the following rewritten paragraph:**

Japanese Patent Application Unexamined Publication No. 2000-347985 discloses a portable radio terminal which is equipped with a main CPU for ~~control~~ controlling the entire operation of the terminal and a sub CPU for monitoring a SLEEP control task.

**Please replace the paragraph at page 3, lines 10-13, with the following rewritten paragraph:**

An object of the present invention is to provide a power supply control device and method, which ~~[[allow]]~~ allows reduced power consumption in a portable communication device equipped with a plurality of controllers.

**Please replace the paragraph at page 8, lines 3-21, with the following rewritten paragraph:**

Referring to FIG. 2, a mobile telephone 20 according to an embodiment of the present invention is equipped with a first controller (here, main CPU) 201 and a second controller (here, sub CPU) 202, which are connected by a DPRAM (Dual Port RAM) 203 so that the main CPU 201 performs control operations including an operation check of the sub CPU 202. The operation check, which will be described later, is to monitor an external communication operation of the sub CPU 202 so as to determine whether the halt time period during which the sub CPU 202 does not perform any external communication control exceeds a predetermined time-out period. The DPRAM 203 has two ports each connected to the main CPU 201 and the

sub CPU 202, allowing the main CPU 201 and the sub CPU 202 to obtain access to the DPRAM 203 concurrently while one is reading data and the other is writing data. Accordingly, the DPRAM 203 is used to transfer data at high speed between the main CPU 201 and the sub CPU 202. The DPRAM 203 has a control memory area which stores an operation check reset flag indicating that the sub CPU 202 is reset by the operation check processing.

**Please replace the paragraph at page 12, lines 1-12, with the following rewritten paragraph:**

Referring to FIG. 4, in the main CPU 201, the sub CPU controller 2b instructs the power supply circuit 208 to supply power to the sub CPU ~~[[201]]~~ 202 and the clock generator to supply timing clock to the sub CPU 202 (step A1). When the sub CPU 202 is in power-on state, the sub CPU controller 2b notifies the EIF task 2a that the sub CPU 202 is powered on and thereby the EIF task 2a instructs the timer handler to start the timer for operation check (step A2). Thereafter, messages are transferred through the DPRAM 203 between the EIF task 2a and the transmission management task 2h and between the transmission management tasks 2d and 2h. Such message transfer is monitored by the DPRAM handlers 2e and 2f.

**Please replace the paragraph from page 13, line 17, to page 14, line 4, with the following rewritten paragraph:**

In the operation check time-out processing (step A7), the EIF task 2a instructs the sub CPU controller 2b to stop supplying the sub CPU 202 with power and timing clock (step A8), sends the transmission management task 2d a message indicating that the sub CPU controller 2b resets the sub CPU 202, and calls on initialization of the DPRAM handler 2e. In addition, the EIF task 2a instructs the DPRAM handler 2e to set the operation check reset flag to "reset by operation check". When the EIF task 2a is notified of the ~~[[cub]]~~ sub CPU 202 being powered off, the EIF task 2a instructs the timer handler 2c to stop the timer for operation check (step A9). When the sub CPU 202 is powered on, the initialization is performed by looking at the operation check reset flag in the DPRAM 203 indicating that the sub CPU 202 has been reset by the operation check.

**Please replace the paragraph at page 14, lines 5-6, with the following rewritten paragraph:**

The operation check request and response processing (steps A 5 and A6) will be described in ~~details~~ detail.